AMENDMENTS TO THE CLAIMS

Please amend the claims as follows:

Listing of Claims:

Claim 1 (Currently Amended): A radio communication control device comprising:

a demodulation unit configured to demodulate a received signal;

a detection circuit, coupled to an output end of the demodulation unit, configured to detect final data contained in a received data stream supplied from the demodulation unit, said detection circuit further configured to output a final data notification signal when detecting the final data; and

a standby period timer, coupled to an output end of the detection circuit, configured to set a standby period in accordance with the final data notification signal output from said detection circuit,

wherein the received data stream includes,

a data section including a plurality of symbols; and

a symbol length indicating the number of symbols included in the data section,

wherein said detection circuit includes,

an arithmetic operation circuit configured to calculate the number of symbols from the symbol length included in the received data stream;

a register configured to hold the number of symbols supplied from said arithmetic operation circuit;

a counter configured to count the number of symbols included in the received data stream; and

a comparator configured to compare the number of symbols counted by the counter and the number of symbols held by the register with each other, said comparator further

configured to output the final data notification signal when these numbers coincide with each other.

Claims 2-3 (Cancelled).

Claim 4 (Previously Presented): The device according to claim 1, wherein the standby period timer is further configured to subtract a start delay time of the standby period timer and a delay time for a data transmission process from a standby period defined by a specification, in accordance with the final data notification signal, and is configured to obtain an actual standby period.

Claim 5 (Previously Presented): The device according to claim 4, wherein the standby period timer further comprises:

a subtracter configured to subtract a start delay time of the standby period timer and a delay time for a data transmission process from a standby period defined by a specification, in accordance with the final data notification signal, and to obtain an actual standby period;

an adder configured to add a present time to the actual standby period supplied from said subtracter; and

a comparator configured to compare the time outputted from the adder and the present time with each other, said comparator further configured to output a signal when both times coincide with each other.

Claim 6 (Currently Amended): The device according to claim [[3]] 1, further comprising:

a buffer circuit connected to an output terminal of the detection circuit, and configured to hold symbols outputted from said detection circuit;

a Viterbi decoder connected to an output terminal of the buffer circuit, and configured to decode the symbols outputted from said detection circuit, to reproduce a frame; and

a receiver unit configured to receive the frame outputted from said Viterbi decoder.

Claim 7 (Original): The device according to claim 1, further comprising:

a transmitter unit connected to the standby period timer, and configured to transmit a frame in accordance with an output signal of the standby period timer.

Claim 8 (Currently Amended): A radio communication control device comprising:

a demodulation unit configured to demodulate a received signal;

a detection circuit, coupled to an output end of the demodulation unit, configured to count the number of symbols contained in a received data stream supplied from said demodulation unit, said detection circuit further configured to output a final data notification signal when the counted number becomes equal to a predetermined symbol number;

a standby period timer, coupled to an output end of the detection circuit, configured to set a standby period in accordance with the final data notification signal output from said detection circuit,

wherein the received data stream includes,

a data section including a plurality of symbols; and

a symbol length indicating the number of symbols included in the data section,

wherein said detection circuit includes,

an arithmetic operation circuit configured to calculate the number of symbols from the symbol length included in the received data stream;

a register configured to hold the number of symbols supplied from the arithmetic

operation circuit;

a counter configured to count the number of symbols included in the received data

stream; and

a comparator configured to compare the number of symbols counted by the counter

and the number of symbols held by the register with each other, said comparator configured

to output the final data notification signal when these numbers coincide with each other.

Claims 9-10 (Cancelled).

Claim 11 (Previously Presented): The device according to claim 8, wherein the

standby period timer is configured to subtract a start delay time of the standby period timer

and a delay time for a data transmission process from a standby period defined by a

specification, in accordance with the final data notification signal, and configured to obtain

an actual standby period.

Claim 12 (Previously Presented): The device according to claim 11, wherein the

standby period timer further comprises:

a subtracter configured to subtract a start delay time of the standby period timer and a

delay time for a data transmission process from a standby period defined by a specification,

in accordance with the final data notification signal, and to obtain an actual standby period;

an adder configured to add a present time to the actual standby period supplied from

the subtracter; and

a comparator configured to compare the time outputted from the adder and the present time with each other, the comparator further configured to output a signal when both times coincide with each other.

Claim 13 (Currently Amended): The device according to claim [[10]] 8, further comprising:

a buffer circuit connected to an output terminal of the detection circuit, and configured to hold symbols outputted from the detection circuit;

a Viterbi decoder connected to an output terminal of the buffer circuit, and configured to decode the symbols outputted from the detection circuit, to reproduce a frame; and

a receiver unit configured to receive the frame outputted from the Viterbi decoder.

Claim 14 (Original): The device according to claim 8, further comprising:

a transmitter unit connected to the standby period timer, and configured to transmit a frame in accordance with an output signal of the standby period timer.

Claim 15 (Currently Amended): A radio communication control device which starts data transmission when a predetermined time elapses after reception of transmission data, said device comprising:

a demodulation unit configured to demodulate a received signal;

a detection circuit, coupled to an output end of the demodulation unit, configured to count the number of symbols contained in a received data stream supplied from said demodulation unit, said detection circuit further configured to output a final data notification signal when the counted number becomes equal to a predetermined symbol number;

a standby period timer, coupled to an output end of the detection circuit, configured to set a standby period in accordance with the final data notification signal output from said detection circuit,

wherein the received data stream includes,

a data section including a plurality of symbols; and

a symbol length indicating the number of symbols included in the data section,

wherein said detection circuit includes,

an arithmetic operation circuit configured to calculate the number of symbols from the symbol length included in the received data stream;

a register configured to hold the number of symbols supplied from the arithmetic operation circuit;

a counter configured to count the number of symbols included in the received data stream; and

a comparator configured to compare the number of symbols counted by the counter and the number of symbols held by the register with each other, said comparator further configured to output the final data notification signal when these numbers coincide with each other.

Claims 16-17 (Cancelled).

Claim 18 (Previously Presented): The device according to claim 15, wherein the standby period timer is configured to subtract a start delay time of the standby period timer and a delay time for a data transmission process from a standby period defined by a specification, in accordance with the final data notification signal, and is configured to obtain an actual standby period.

Claim 19 (Previously Presented): The device according to claim 18, wherein the standby period timer further comprises:

a subtracter configured to subtract a start delay time of the standby period timer and a delay time for a data transmission process from a standby period defined by a specification, in accordance with the final data notification signal, and to obtain an actual standby period;

an adder configured to add a present time to the actual standby period supplied from the subtracter; and

a comparator configured to compare the time outputted from the adder and the present time with each other, the comparator further configured to output a signal when both times coincide with each other.

Claim 20 (Original): The device according to claim 15, further comprising:

a buffer circuit connected to an output terminal of the detection circuit, and configured to hold symbols outputted from the detection circuit;

a Viterbi decoder connected to an output terminal of the buffer circuit, and configured to decode the symbols outputted from the detection circuit, to reproduce a frame; and

a frame receiver unit configured to receive the frame outputted from the Viterbi decoder.